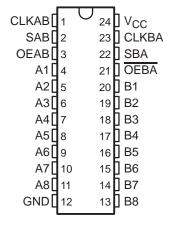
- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Power-Up High-Impedance Mode
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic and Ceramic 300-mil DIPs (JT, NT)

description

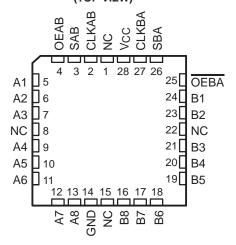
These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Output-enable (OEAB and OEBA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'BCT652.

SN54BCT652...JT OR W PACKAGE SN74BCT652...DW OR NT PACKAGE (TOP VIEW)



SN54BCT652...FK PACKAGE (TOP VIEW)



NC - No internal connection

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration each output reinforces its input. Therefore, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remain at its last state.

The SN54BCT652 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74BCT652 is characterized for operation from 0°C to 70°C.

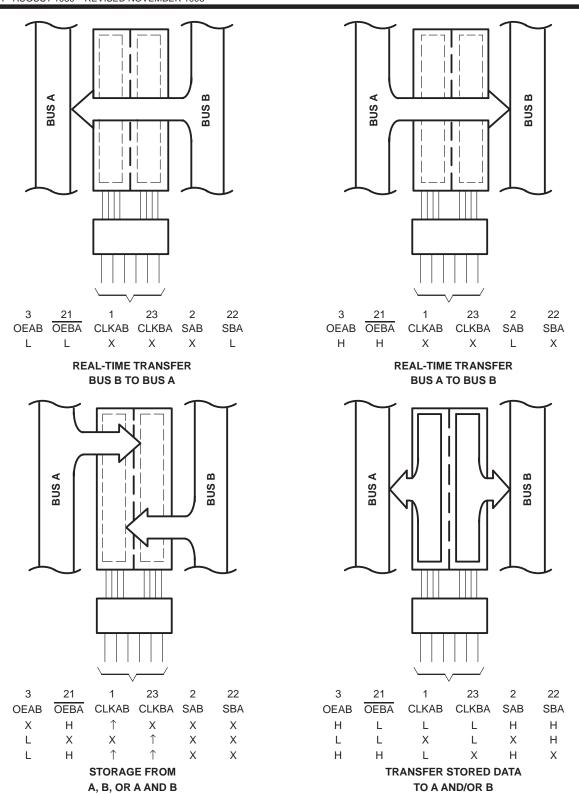


Figure 1. Bus-Management Functions

Pin numbers shown are for the DW, JT, NT, and W packages.

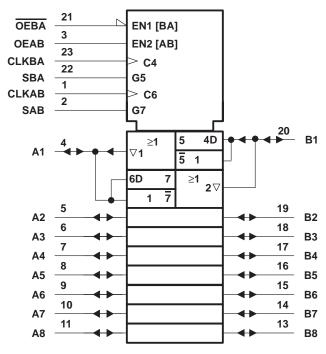


FUNCTION TABLE

		INPU ⁻	гѕ			DATA	A 1/0†	OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
L	Н	H or L	H or L	Х	Х	Input	Input	Isolation
L	Н	\uparrow	\uparrow	X	X	Input	Input	Store A and B data
X	Н	\uparrow	H or L	X	X	Input	Unspecified [‡]	Store A, hold B
Н	Н	\uparrow	\uparrow	X‡	X	Input	Output	Store A in both registers
L	X	H or L	\uparrow	X	X	Unspecified [‡]	Input	Hold A, store B
L	L	\uparrow	\uparrow	X	X‡	Output	Input	Store B in both registers
L	L	Χ	Χ	X	L	Output	Input	Real-time B data to A bus
L	L	Χ	H or L	X	Н	Output	Input	Stored B data to A bus
Н	Н	X	Χ	L	X	Input	Output	Real-time A data to B bus
Н	Н	H or L	Χ	Н	X	Input	Output	Stored A data to B bus
н	L	H or L	H or L	Н	Н	Output	Output	Stored A data to B bus and stored B data to A bus

[†] The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

logic symbol§

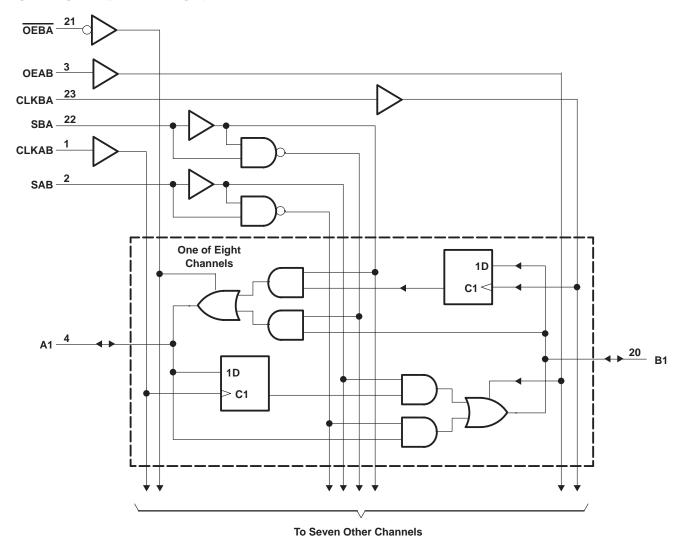


§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DW, JT, NT, and W packages.

[‡] Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered in order to load both registers.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, NT, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		– 0.5 V to 7 V
Input voltage range: Control inputs (see	Note 1)	– 0.5 V to 7 V
I/O ports (see Note	1)	– 0.5 V to 5.5 V
Voltage range applied to any output in the	ne disabled or power-off state, VO	– 0.5 V to 7 V
Voltage range applied to any output in the	ne high state, VO	– 0.5 V to V _{CC}
Current into any output in the low state: \$	SN54BCT652	96 mÅ
	SN74BCT652	128 mA
Operating free-air temperature range: \$	SN54BCT652	– 55°C to 125°C
	SN74BCT652	0°C to 70°C
Storage temperature range		– 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.



recommended operating conditions

		SN	54BCT6	52	SN	74BCT6	52	UNIT
			NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
ΙΙΚ	Input clamp current			-18			-18	mA
IOH	High-level output current			-12			-15	mA
lOL	Low-level output current			48			64	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

D	ARAMETER	TEC	TEST CONDITIONS			52	SN	74BCT6	52	UNIT
Ρ/	ARAWETER	TES				MAX	MIN	TYP†	MAX	UNII
VIK		$V_{CC} = 4.5 \text{ V},$	$I_{I} = -18 \text{ mA}$			-1.2			-1.2	V
			$I_{OH} = -3 \text{ mA}$	2.4	3.3		2.4	3.3		
Vон		V _{CC} = 4.5 V	$I_{OH} = -12 \text{ mA}$	2	3.2					V
			$I_{OH} = -15 \text{ mA}$				2	3.1		
V/01		V _{CC} = 4.5 V	I _{OL} = 48 mA		0.38	0.55				V
VOL	VOL VCC =		$I_{OL} = 64 \text{ mA}$					0.42	0.55	V
1.	A or B port	V00 - 5 5 V	V _I = 5.5 V			1			1	mA
lı .	Control inputs	V _{CC} = 5.5 V,	V = 5.5 V			1			1	IIIA
ı†	A or B port	V00 - 5 5 V	V _I = 2.7 V			70			70	
¹ıн [‡]	Control inputs	V _{CC} = 5.5 V,	V = 2.7 V		20		20	μΑ		
ı. t	A or B port	V00 - 5 5 V	V _I = 0.5 V			-0.7			-0.7	mA
I _{IL} ‡	Control inputs	V _{CC} = 5.5 V,	V = 0.5 V		-0.7			-0.7		
los§		V _{CC} = 5.5 V,	V _O = 0	-100		-225	-100		-225	mA
ICCL	A or B port	$V_{CC} = 5.5 V,$	V _I = 0		43	69		43	69	mA
ICCH	A or B port	V _{CC} = 5.5 V,	V _I = 4.5 V		6	10		6	10	mA
ICCZ	A or B port	V _{CC} = 5.5 V,	V _I = 0		10	17		10	17	mA
Ci	Control inputs	V _{CC} = 5 V,	V _I = 2.5 V or 0.5 V		6			6		pF
Cio	A or B port	V _{CC} = 5 V,	V _O = 2.5 V or 0.5 V		14			14		pF

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		V _{CC} = 5 V, T _A = 25°C		SN54B	CT652	SN7BC	UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	0	77	0	77	0	77	MHz
t _W	Pulse duration, CLK high or low	6.5		7		6.5		ns
t _{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	5		6		5		ns
t _h	Hold time, A or B after CLKAB↑ or CLKBA↑	1		1		1		ns



[†] All typical values are at V_{CC} = 5 V, T_A = 25°C. ‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

SN54BCT652, SN74BCT652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS038A - AUGUST 1989 - REVISED NOVEMBER 1993

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		CC = 5 V A = 25°C		SN54B	CT652	SN74B	CT652	UNIT
	(INPUT)	(001701)	MIN	TYP	MIN	MIN	MAX	MIN	MAX	
f _{max}			77			77		77		MHz
^t PLH	CLKBA	А	2.6	6.9	8.9	2.6	11.6	2.6	10.5	ne
^t PHL	CLNDA	^	2.8	6.8	8.8	2.8	10.7	2.8	9.9	ns
^t PLH	CLKAB	В	2.6	6.9	8.9	2.6	11.6	2.6	10.5	ns
^t PHL	CENAB	Ь	2.8	6.8	8.8	2.8	10.7	2.8	9.9	113
^t PLH	А	В	1.7	5.8	7.5	1.7	10.3	1.7	8.9	ns
^t PHL	^	Ь	2.4	6.5	8.2	2.4	11	2.4	9.8	113
^t PLH	В	А	1.7	5.8	7.5	1.7	10.3	1.7	8.9	ne
^t PHL	В	^	2.4	6.5	8.2	2.4	11	2.4	9.8	ns
^t PLH	SBAT	А	3.5	8.8	10.8	3.5	14.2	3.5	13.1	ns
^t PHL	(with B high)	^	2.4	5.9	7.7	2.4	9.1	2.4	8.5	
^t PLH	SBAT	А	3	7.6	9.7	3	12.4	3	11.3	ns
^t PHL	(with B low)	^	3.8	8.3	10.4	3.8	12.9	3.8	12.5	
^t PLH	SABŤ	В	3.5	8.8	10.8	3.5	14.2	3.5	13.1	ns
^t PHL	(with A high)	Ь	2.4	5.9	7.7	2.4	9.1	2.4	8.5	115
^t PLH	SABŤ	В	3	7.6	9.7	3	12.4	3	11.3	ne
^t PHL	(with A low)	Ь	3.8	8.3	10.4	3.8	12.9	3.8	12.5	ns
^t PZH	OEBA	А	2.5	7.2	8.9	2.5	11.2	2.5	10.6	ne
^t PZL	OEBA	^	3.2	8.1	10.1	3.2	12.6	3.2	12	ns
^t PHZ	OEBA	А	2.8	6.7	8.6	2.8	10.9	2.8	10	ns
t _{PLZ}	OEBA	^	2.4	6.3	8.4	2.4	10.5	2.4	9.5	113
^t PZH	OEAB	В	1.5	5.4	7.1	1.5	9	1.5	8.1	ns
^t PZL	OLAD		2.3	6.2	8.1	2.3	10.3	2.3	9.3	113
^t PHZ	OEAB	В		8.2	10	3.5	12.2	3.5	11.6	ne
^t PLZ	OLAD		2.8	7.2	9.5	2.8	12	2.8	11.3	ns

[†] These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

PACKAGE OPTION ADDENDUM



18-Sep-2008

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9155301M3A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9155301MKA	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9155301MLA	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type
SN74BCT652DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT652DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT652DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT652DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT652DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT652DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT652NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74BCT652NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SNJ54BCT652FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54BCT652JT	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54BCT652W	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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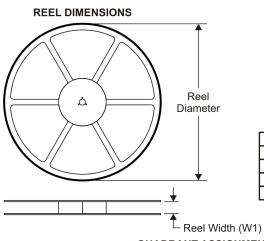
PACKAGE OPTION ADDENDUM

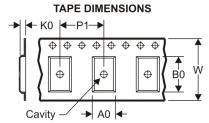
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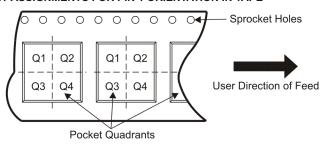
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74BCT652DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1





*All dimensions are nominal

ĺ	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
	SN74BCT652DWR	SOIC	DW	24	2000	346.0	346.0	41.0

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES: A. All linear dimensions are in inches (millimeters).

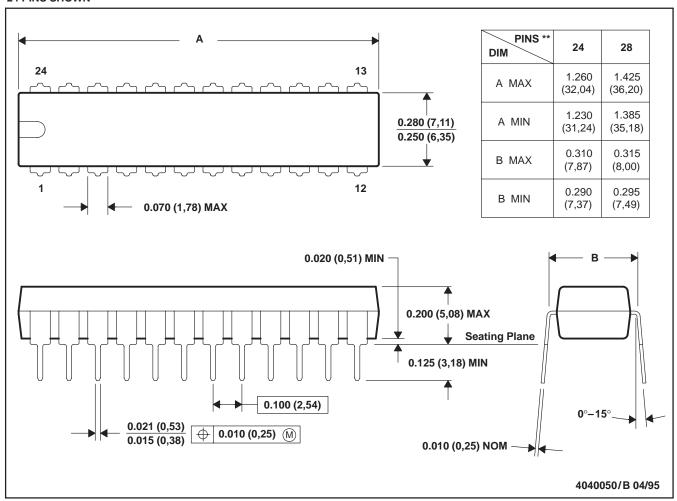
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004



NT (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

DW (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.



W (R-GDFP-F24)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
 - E. Index point is provided on cap for terminal identification only.



JT (R-GDIP-T**)

24 LEADS SHOWN

CERAMIC DUAL-IN-LINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

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